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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,713	01/06/2004	Daniel C. Edelstein	FIS920030255US1	1712

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,713	EDELSTEIN ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *17-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/707713 Attorney's Docket #: FIS920030255US1
Filing Date: 1/6/2004;

Applicant: Edelstein et al.

Examiner: Alexander Williams

Applicant's Amendment filed 5/6/05 and 2/4/05 to the election of Group I (claims 1 to 16), filed 8/19/04, has been acknowledged.

This application contains claims 17 to 31 drawn to an invention non-elected without traverse.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the substrate; a plurality of integrated circuit chips fabricated on said substrate in claim 1 and said semiconductor wafer comprises a plurality of layers of said at least one second dielectric material 15; and at least one of said layers of second dielectric material is SiO2 and at least one of said layers of second dielectric material is SiNx in claim 16 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claims 1 to 16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is unclear and confusing to what is meant by and what shows "a semiconductor wafer comprising: **a substrate**; a plurality of **integrated circuits chips** fabricated on said substrate; a dicing channel disposed between adjacent ones of said **integrated circuits chips**, said channel exposing sidewalls **of said integrated circuits**; a layer of first dielectric material disposed on a top surface and sidewalls of said integrated circuits chips; and at least one layer of at least one second dielectric material disposed on said layer of first dielectric material." The phrase "said channel exposing sidewalls **of said integrated circuits"** should also have chips added. Also, "integrated circuits chips" should be –integrated circuit chips--. Figure 1 does show a plurality of integrated circuit chips on a substrate. In figure 2, how is "a substrate; **a plurality of integrated circuit chips fabricated on said substrate**?"

In claim 15, it is unclear and confusing to what is meant by and what shows "said semiconductor wafer comprises a plurality of layers of said at least one second dielectric material." Where is this shown in the drawing?

In claim 16, it is unclear and confusing to what is meant by and what shows "at least one of said layers of second dielectric material is SiO2 and at least one of said layers of second dielectric material is SiNx. Where is this shown in the drawing?

Any of claims 1 to 16 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 12, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Massginill et al. (U.S. Patent # 6,882,045 B2).
1. Massginill et al. (figures 76 to 87) specifically figure 76 show a semiconductor wafer **410** comprising: a substrate **411**; a plurality of integrated circuits chips **442** fabricated on said substrate; a dicing channel **490** disposed between adjacent ones of said integrated circuits chips, said channel exposing sidewalls of said integrated circuits; a layer of first dielectric material disposed on a top surface and sidewalls of said integrated circuits chips; and at least one layer of at least one second dielectric material disposed on said layer of first dielectric material, wherein said first dielectric material has a Gc value of at least about 10 times greater than said second dielectric material (inherit since the same material are used).
2. The semiconductor wafer of Claim 1, Massginill et al. show wherein said first dielectric material has a Gc value greater than about 0.1 kj/m2 (inherit since the same material are used).
3. The semiconductor wafer of Claim 1, Massginill et al. show wherein said first dielectric material has a Gc value of about 0.5 to about c 2.5 kj/m2 (inherit since the same material are used).
4. The semiconductor wafer of Claim 1, Massginill et al. show wherein said second dielectric material has a Gc value less than about c 0.05 kj/mz (inherit since the same material are used).
5. The semiconductor wafer of Claim 1, Massginill et al. show wherein said second dielectric material has a G value of about 0.005 to c about 0.05 kJ/m2 (inherit since the same material are used).
6. The semiconductor wafer of Claim 1, Massginill et al. show wherein said first dielectric material has a tensile strength of about 20 to 100 Mpa (inherit since the same material are used).
7. The semiconductor wafer of Claim 1, Massginill et al. show wherein said second dielectric material has a tensile strength of about 700 to 10, 000 M Pa (inherit since the same material are used).
As to claims 2 to 8, Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom.

Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. The semiconductor wafer of Claim 1, Massginill et al. show wherein said first dielectric material is selected from the group consisting of polyesters, phenolics, **polyimides**, polysulfones, polyether ether ketones, polyurethanes, epoxies, polyarylene ethers, and polyethylene terepthalates.

9. The semiconductor wafer of Claim 1, Massginill et al. show wherein said a dielectric material is a polyarylene ether.

10. The semiconductor wafer of Claim 1, Massginill et al. show wherein said second dielectric material is selected from the group consisting of SiNX, SiOz, SiC, TEOS, FTEOS, **FSG**, and **OSG**.

11. The semiconductor wafer of Claim 1, Massginill et al. show wherein said second dielectric material is SiO2.

12. The semiconductor wafer of Claim 1, Massginill et al. show wherein said dicing channel exposes sidewalls of said integrated circuits and sidewalls of said substrate.

[0105] Suitable dielectric material(s) include B-stage polymeric compounds, such as polyimides, epoxy resins, polyurethanes or silicons, provided that these compounds are produced with a low dielectric constant at 20.degree. C. Additional suitable materials could include thermosetting materials, such as high glass transition anhydride-cured epoxy composition possessing a low dielectric constant at 20.degree. C. More particular suitable thermoset materials include, but are not limited to, one or more compounds produced with a low dielectric constant at 20.degree. C. and selected from group consisting of epoxies and modified epoxies, melamine-formaldehydes, urea formaldehydes, phelonic resins, poly(bis-maleimides), acetylene-terminated BPA resins, IPN polymers, triazine resins, and mixtures thereof. Further additional suitable materials include high temperature thermoplastic materials, such as liquid crystal polyesters (e.g., Xydar.TM. or Vectra.TM.), poly-(ether ether ketones), or the poly(aryl ether ketones), provided that these thermoplastic materials are produced such as to possess the low dielectric constant at 20.degree. C. Additional suitable thermoplastic materials include, by way of example only, ABS-containing resinous materials (ABS/PC, ABS/polysulfone, ABS/PVC), acetals acrylics, alkyds, allylic ethers, benzocyclobutenes, cellulosic esters, chlorinated

polyalkylene ethers, cyanate, cyanamides, furans, parylene amorphous fluoropolymers, polyalkylene ethers, polyamides (Nylons), polyarylene ethers, perfluoroalkoxy polymeric resins, fluoroethylenepropylene polymers, polybutadienes, polycarbonates, polyesters, polyfluorocarbons, polyimides, polyphenylenes, polyphenylene sulfides, polypropylenes, polystyrenes, polysulfones, polyurethanes, polyvinyl acetates, polyvinyl chlorides, polyvinyl chloride/vinylidine chlorides, polyetherimides, and the like, and mixtures of any of the foregoing, provided that the materials are manufactured to have a low dielectric constant at 20.degree. C.

[0106] In another preferred embodiment of the invention the low dielectric constant material comprises a polymer having the repeat structure (--CH.sub.2C.sub.6H.sub.4CH.sub.2--).sub.n wherein n is an integer having a value ranging from about 2,000 to about 8,000; more preferably from about 3,000 to about 7,000; most preferably from about 4,000 to about 6,000, such as from about 4,500 to about 5,500 including from about 4,800 to about 5,200. In a further embodiment of the invention the low dielectric constant material comprises the repeat structure (--CF.sub.2--CF.sub.2--).sub.n wherein n is an integer having a value ranging from about 3,000 to about 16,000; more preferably from about 4,000 to about 14,000; most preferably from about 8,000 to about 12,000.

[0178] Referring now to FIGS. 76-87, there is seen an exemplary multichip module with capacitor structures, generally illustrated as 410 in FIG. 76. To simplify the visual presentation of module 410, only a cross-sectional slice of the module is shown in the Figures, with it being understood that additional portions of the module lie to the left of the left straight edge of the slice and to the right of the right straight edge of the slice. Substrate 410 comprises a primary substrate 411 which is affixed to a secondary substrate 470 by an adhesive layer 480. Primary substrate 411 preferably comprises a silicon wafer, and secondary substrate 470 preferably comprises a ceramic substrate. Adhesive layer 480 may comprise a bonding sheet (also called a bonding film), and examples thereof are described in greater detail below. Several dielectric and conductive layers are formed on top of primary substrate 411, ending with a plurality of conductive interconnect pads 461 at the top of module 410. Among other purposes, some of the pads 461 are used to interconnect to one or more integrated circuit chips 442, each of which has a

plurality of corresponding interconnect pads 443. The interconnection of the pads 461 and 443 is preferably made by way of a plurality of reflowed solder bumps 445, such an may be formed in a conventional flip-chip bounding process.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of layers deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 1 to 8 and 10 to 16, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over by Farnworth et al. (U.S. Patent # 5,786,632).

1. Farnworth et al. (figures 1 to 6) specifically figure 3 show a semiconductor wafer **10**comprising: a substrate **46**; a plurality of integrated circuits **30** fabricated on said substrate; a dicing channel **44** disposed between adjacent ones of said integrated circuits, said channel exposing sidewalls of said integrated circuits; a layer of first dielectric material **36** disposed on a top surface and sidewalls of said integrated circuits; and at least one layer of at least one second dielectric material **36** disposed on said layer of first dielectric material, wherein said first dielectric material has a Gc value of at least about 10 times greater than said second dielectric material (inherit since the same material are used).

2. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said first dielectric material has a Gc value greater than about 0.1 kj/m2 (inherit since the same material are used).

3. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said first dielectric material has a Gc value of about 0.5 to about c 2.5 kj/m2 (inherit since the same material are used).

4. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said second dielectric material has a Gc value less than about c 0.05 kj/mz (inherit since the same material are used).

5. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said second dielectric material has a G value of about 0.005 to c about 0.05 kJ/m2 (inherit since the same material are used).

6. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said first dielectric material has a tensile strength of about 20 to 100 Mpa (inherit since the same material are used).

7. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said second dielectric material has a tensile strength of about 700 to 10, 000 M Pa (inherit since the same material are used).

As to claims 2 to 8, Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions

are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

8. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said first dielectric material is selected from the group consisting of polyesters, phenolics, **polyimides**, polysulfones, polyether ether ketones, polyurethanes, epoxies, polyarylene ethers, and polyethylene terepthalates.

10. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said second dielectric material is selected from the group consisting of SiNX, **SiOz**, SiC, TEOS, FTEOS, FSG, and OSG.

11. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said second dielectric material is SiO2.

12. The semiconductor wafer of Claim 1, Farnworth et al. show wherein said dicing channel exposes sidewalls of said integrated circuits and sidewalls of said substrate.

(5) Conventionally, semiconductor dice are formed on a wafer of silicon material that is diced to form multiple bare dice.

3) In accordance with the invention, an additional protective layer 36 and pattern of conductive traces 38 are formed on the face of the die 30. The protective layer 36 and conductive traces 38 can also be formed at the wafer level prior to dicing of the wafer. The protective layer 36 is formed over the conventional circuitry 48 and covers the face of the die 30. The protective layer 36 can be formed of an electrically insulating material such as a polyimide, borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), TEOS (deposited by the decomposition of tetraethyl orthosilicate), a nitride (e.g., Si.sub.3 N.sub.4) or an oxide (e.g., SiO.sub.2).

(13) The cover 72 (FIG. 5) is adapted to be attached to the base 74 to retain the dice 30 within the die cavities 76. The cover 72 can be attached to the base 74 using a suitable adhesive such as a curable epoxy. In addition, the cover 72 can include a resilient biasing pad as described in the above cited U.S. Patent application to help maintain the die 30 in contact with the connector 90.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a plurality of layers deals with an issue (i.e., the

integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 13 to 16, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over by Massginill et al. (U.S. Patent # 6,882,045 B2).

13. The semiconductor wafer of Claim 1, Massginill et al. further comprising a plurality of conductors embedded in said first dielectric material and said second dielectric material and in contact with said plurality of integrated circuits.

14. The semiconductor wafer of Claim 13, Massginill et al. show wherein said conductors are S-shaped or spring shaped or jogged (Same as so far as Applicant's show).
15. The semiconductor wafer of Claim 1, Massginill et al. show wherein said semiconductor wafer comprises a plurality of layers of said at least one second dielectric material.

Therefore, it would have been obvious to one of ordinary skill in the art to use the plurality of layers as "merely a matter of obvious engineering choice" as set forth in the above case law.

Claims 9, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnworth et al. (U.S. Patent # 5,786,632) in view of Sun et al. (U.S. Patent Application Publication # 2003/0222330 A1).

Farnworth et al. show the features of the claimed invention as detail above, but fail to explicitly show wherein said first dielectric material is a polyarylene ether.

Sun et al. is cited for show a passivation processing over a memory link. Specifically, Sun et al. (figures 1 to 11C) specifically figure 3C discloses a dielectric material is a polyarylene ether **46** for the purpose of preventing defects resulting from alignment variations of subsurface layers or patterns contaminated.

Therefore, it would have been obvious to one of ordinary skill in the art to use Sun et al.'s polyarylene ether dielectric material to modify Farnworth et al.'s dielectric material for the purpose of preventing defects resulting from alignment variations of subsurface layers or patterns contaminated.

Response

Applicant's arguments filed 5/6/05 and 2/4/05 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/788,789,790,787,758,700,701,620	11/1/04 7/22/05
Other Documentation: foreign patents and literature in 257/788,789,790,787,758,700,701,620	11/1/04 7/22/05
Electronic data base(s): U.S. Patents EAST	11/1/04 7/22/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams

Primary Examiner
Art Unit 2826

AOW
7/21/05